Code No : **20EC2T03**

R20

I B.TECH II SEMESTER REGULAR EXAMINATIONS, SEPTEMBER - 2021
DIGITAL LOGIC DESIGN
(Common to CSE, IT, AID, CIC, CSM and CSO)

Time: 3 Hours **Max. Marks:70**

Note : Answer **ONE** question from each unit **(5 ×14 = 70 Marks)**

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UNIT-I

1. a) Produce a graphical realization of NOT, AND, OR and XOR using NAND and NOR gates. [8M]

   b) Perform the subtraction with following decimal numbers using 10's complement and 9's complement respectively. (*i).* 5294 – 749, (*ii*) 27 – 289. [6M]

(OR)

2. a) Convert the following expressions into their respective connical forms: [7M]
   $F_1 = AC + \bar{A}BD + AC\bar{D}$, $F_2 = (A + B + \bar{C})(A + D)$

   b) Complete the addition using Excess-3 code for following: [7M]
   (i) 761+455, (ii) 1221 + 565

UNIT-II

3. a) Use a K-map to simplify each of the following two logic expressions as much as possible: [7M]
   $G = \bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + +X\bar{Y}\bar{Z} + \bar{X}\bar{Y}\bar{Z} + XY\bar{Z}$
   $H = \bar{A}\bar{B}CD + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + AB\bar{C}D + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D + ABCD$

   b) Consider the function $z = f(x, y, w, v) = (x.v + \bar{x}.w).\bar{y}.(w + y.\bar{v})$, Draw a schematic diagram for a circuit which would implement this function. [7M]

(OR)

4. a) For the following function F = Σm(1,5,7,8,10,13,14), identify the prime implicants and essential prime implicants. [7M]

   b) Simplify the Boolean function F using the don't care conditions D, in SOP [7M]
   $F = \bar{w}(\bar{x}y + \bar{x}\bar{y} + xyz) + \bar{x}\bar{z}(y + w)$, $D = \bar{w}x(\bar{y}z + y\bar{z}) + wyz$

UNIT-III

5. a) Write and show details of Full adder and Full subtractor. [7M]

   b) Design a BCD - to - Gray code converter using 8:1 multiplexers. [7M]

(OR)

6. a) Implement the Boolean function $F(A, B, C) = \sum m(1,2,4,7)$ using PROM. [7M]

   b) Differentiate between PROM, PAL and PLA. [7M]

UNIT-IV

7. a) Design and explain operation of basic ring and twisted ring counter [7M]

   b) Explain the parallel input serial output shift register. [7M]

(OR)
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8. a) Explain the master-slave flip-flop constructed from two JK flip-flops. [7M]
   b) Show the conversion of D flip-flop into T and JK flip-flops. [7M]

UNIT-V

9. a) Explain the differences between Melay and Moore State machines. [7M]
   b) Draw the Moore type state diagram and state table to detect the sequence 1110. [7M]

(OR)

10. a) Discuss limitations of FSM with suitable example. [7M]
    b) Draw the Melay type state diagram and state table to detect the sequence 1011. [7M]

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